**Files**:

Processor.v

Processor\_tb.v

Control\_unit.v

Instruction Fetch

IF.v

IF\_tb.v

IF\_tb.vcd

IF\_tb.vvp

instrn\_mem.txt/ ISA1.txt

Instruction\_mem.v

Instruction Decode

Reg\_file.v

Reg\_file\_tb.v

Control\_unit.v

Sign\_ext.v

ID.v

EX

Alu.v

Alu\_control.v

EX.v

MEM

MEM.v

MEM\_tb.v

MEM.vvp

MEM.vcd

WB

WB.v

Previous version of project

Contains all the necessary working files of the project including the above ones which was fixed for the last presentation.

Project in progress

Ongoing updates in the project.

**Links Referred:**

* <https://twilco.github.io/riscv-from-scratch/2019/03/10/riscv-from-scratch-1.html>
* <https://www.semanticscholar.org/paper/RVCoreP-%3A-An-optimized-RISC-V-soft-processor-of-Miyazaki-Kanamori/a647632e20e6dae839b1a4f10a581530da45e8e7>
* <http://www.iraj.in/journal/journal_file/journal_pdf/1-378-15037310331-7.pdf>

Vinay Reddy Paper

* YAGS Branch Prediction: <https://people.eecs.berkeley.edu/~kubitron/courses/cs252-F99/handouts/papers/mudge_yags.pdf>
* Dynamic Branch Prediction: <https://www.cse.iitk.ac.in/users/biswap/CS422/L9-BP.pdf>